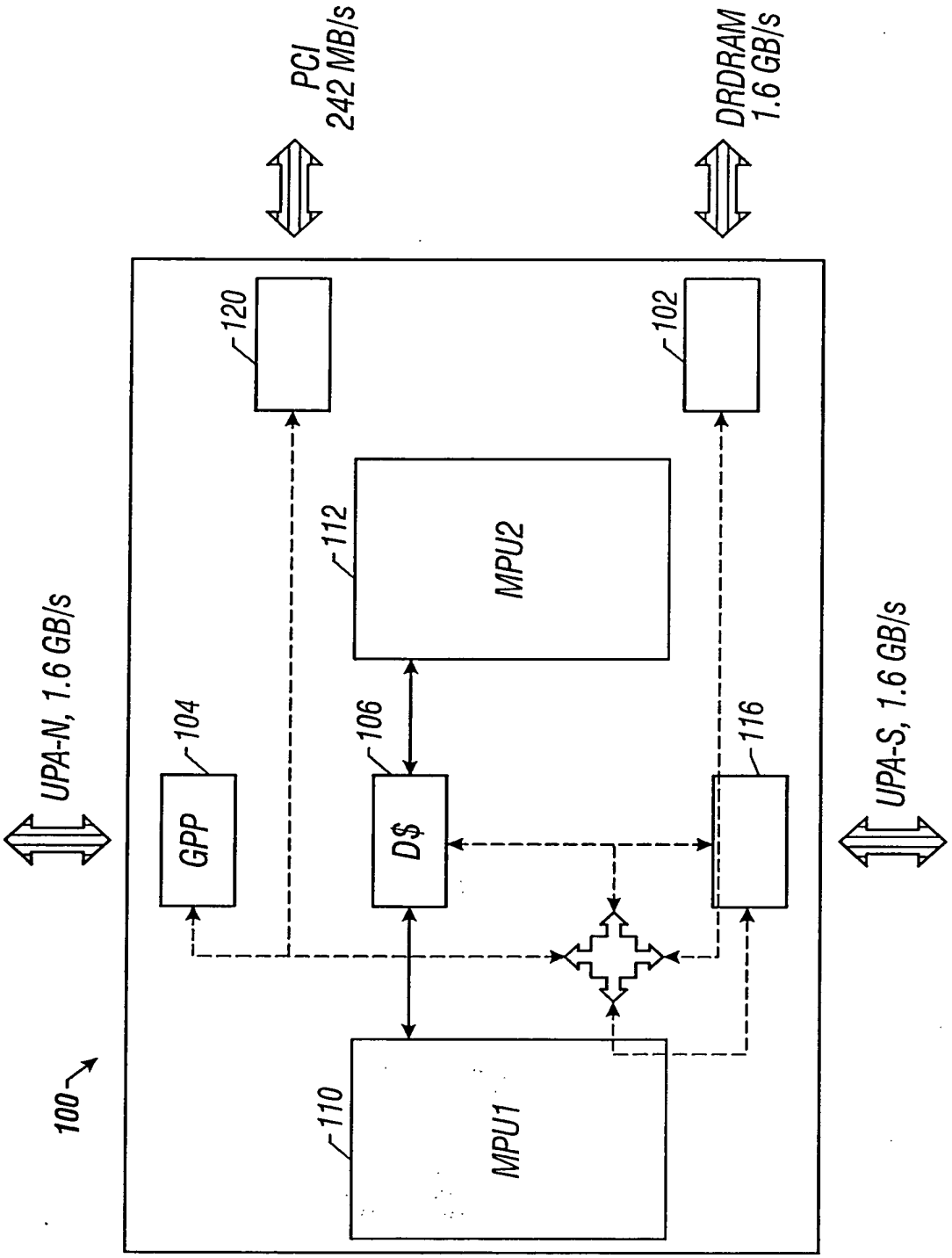
PCI
242 MB/s
DRDRAM
1.6 GB/s
120
102
112
MPU2
UPA-N, 1.6 GB/s
104
106
116
GPP
D$
UPA-S, 1.6 GB/s
100
110
MPU1

FIG. 1

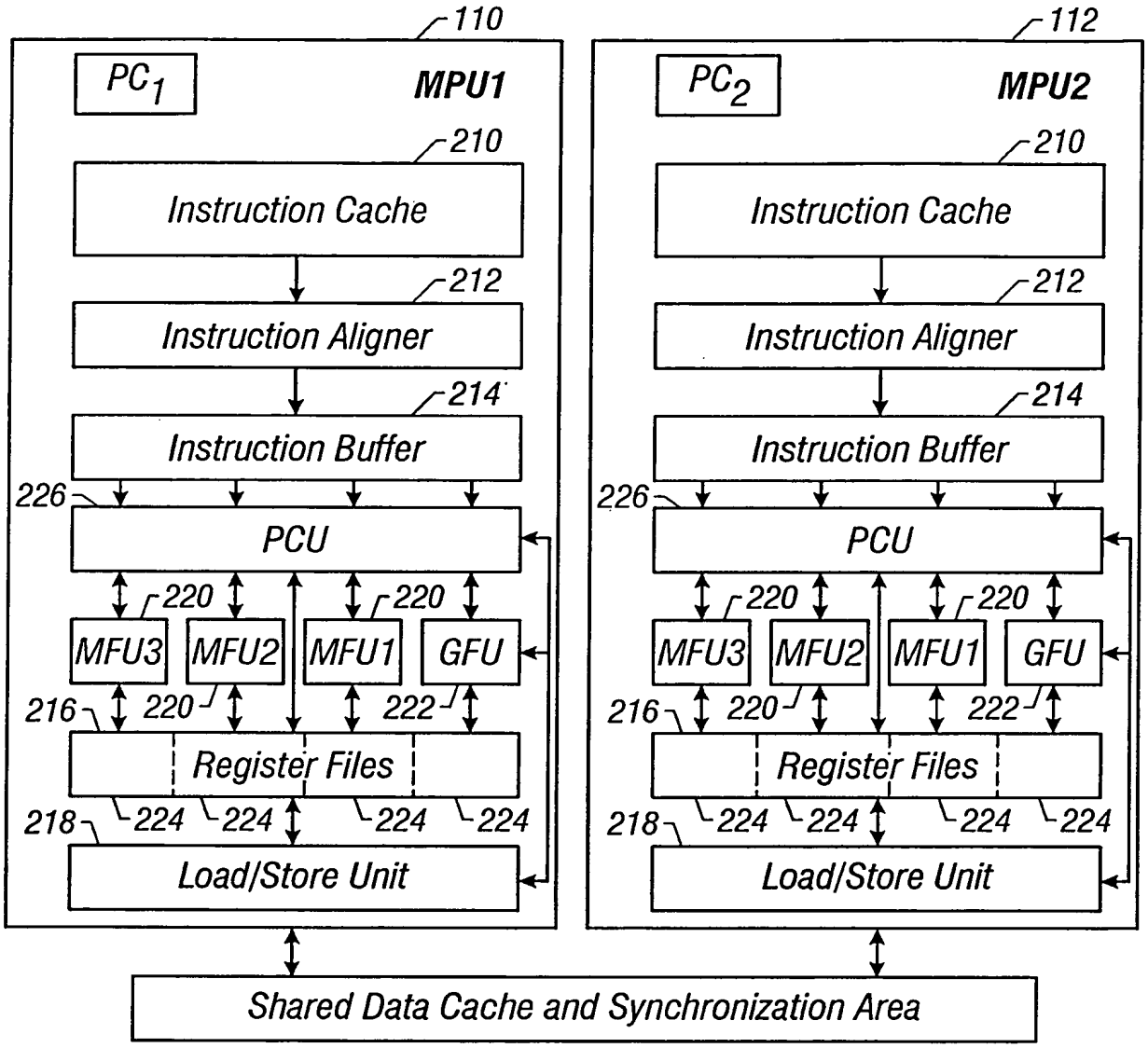
110
112
PC1
MPU1
PC2
MPU2
210
Instruction Cache
212
Instruction Aligner
214
Instruction Buffer
226
PCU
220
MFU3
MFU2
MFU1
GFU
216
222
Register Files
218
224
Load/Store Unit
Shared Data Cache and Synchronization Area

FIG. 2

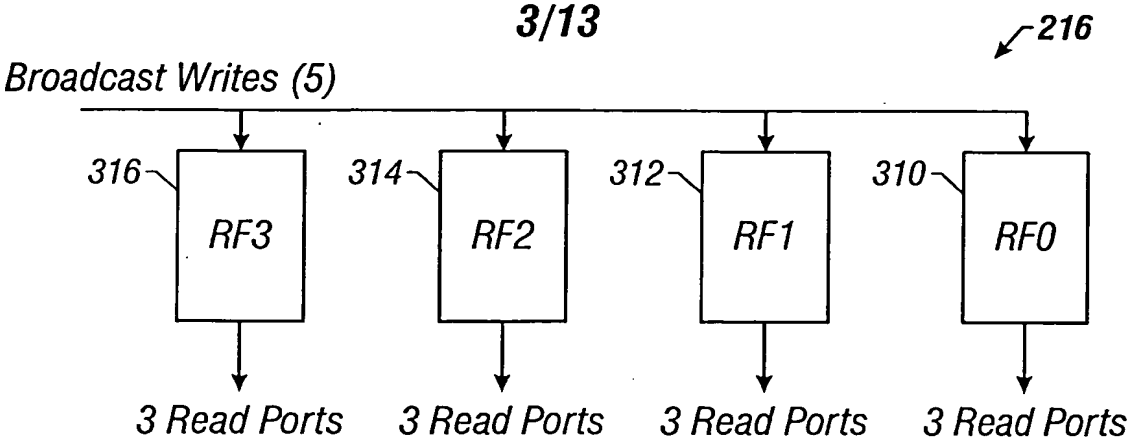

FIG. 3

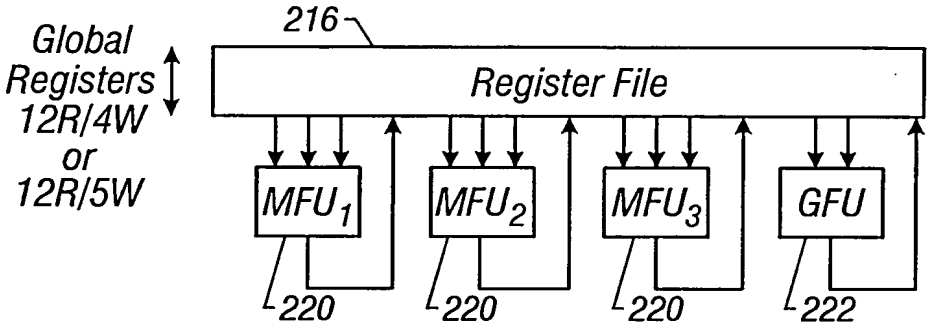

FIG. 4

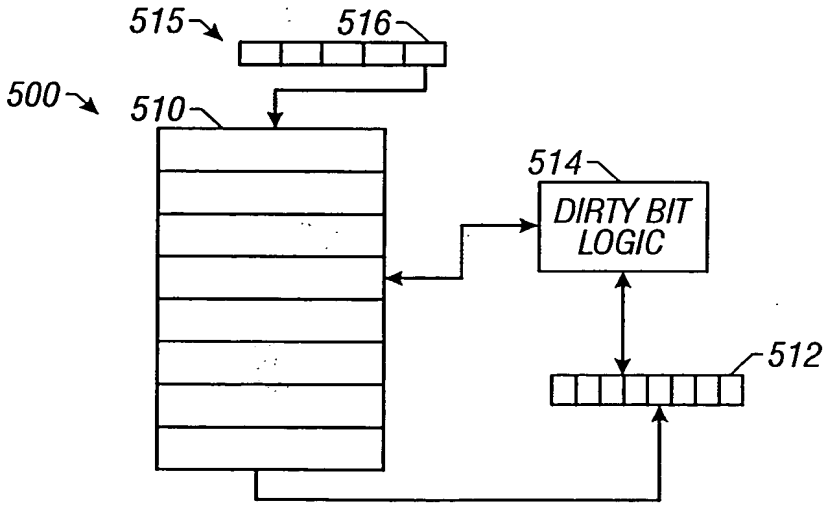

FIG. 5

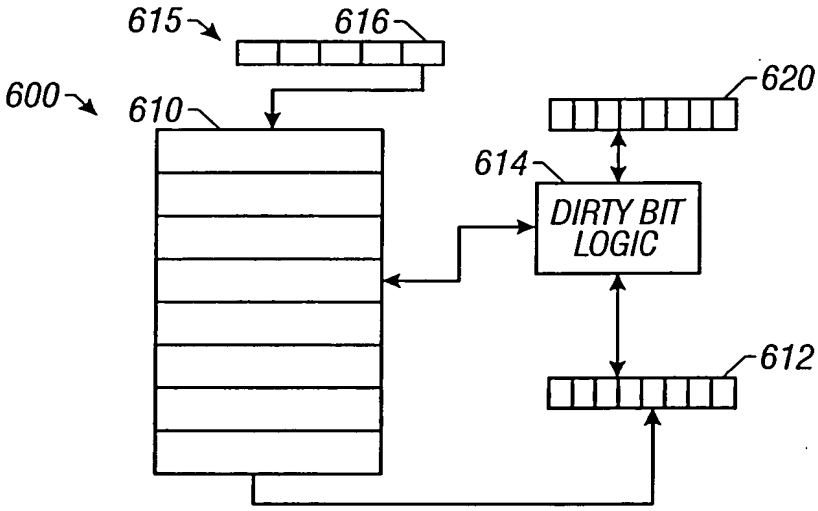
615
616
600
610
620
614
DIRTY BIT LOGIC
612

FIG. 6

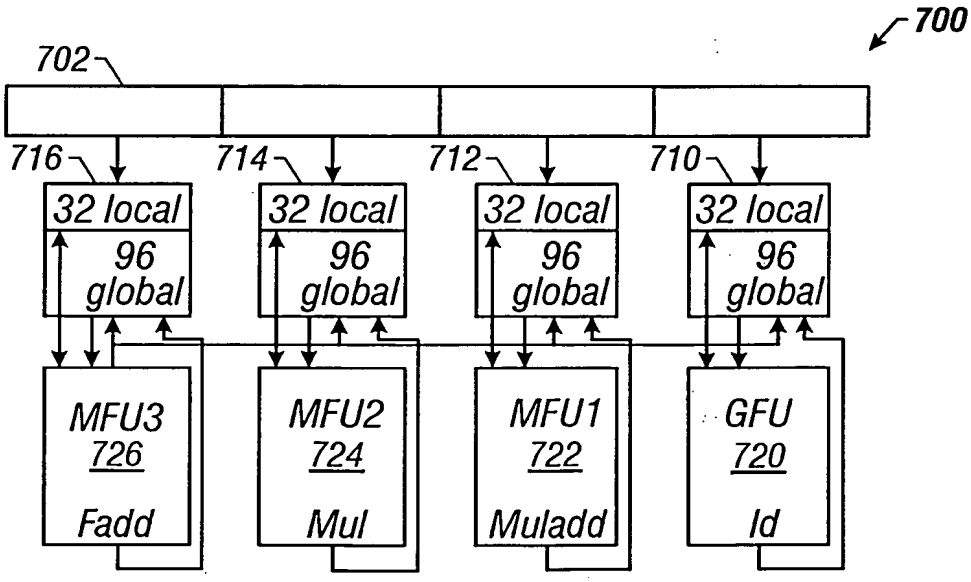
700
702
716
714
712
710
32 local
96 global
32 local
96 global
32 local
96 global
32 local
96 global
MFU3
726
Fadd
MFU2
724
Mul
MFU1
722
Muladd
GFU
720
ld

FIG. 7

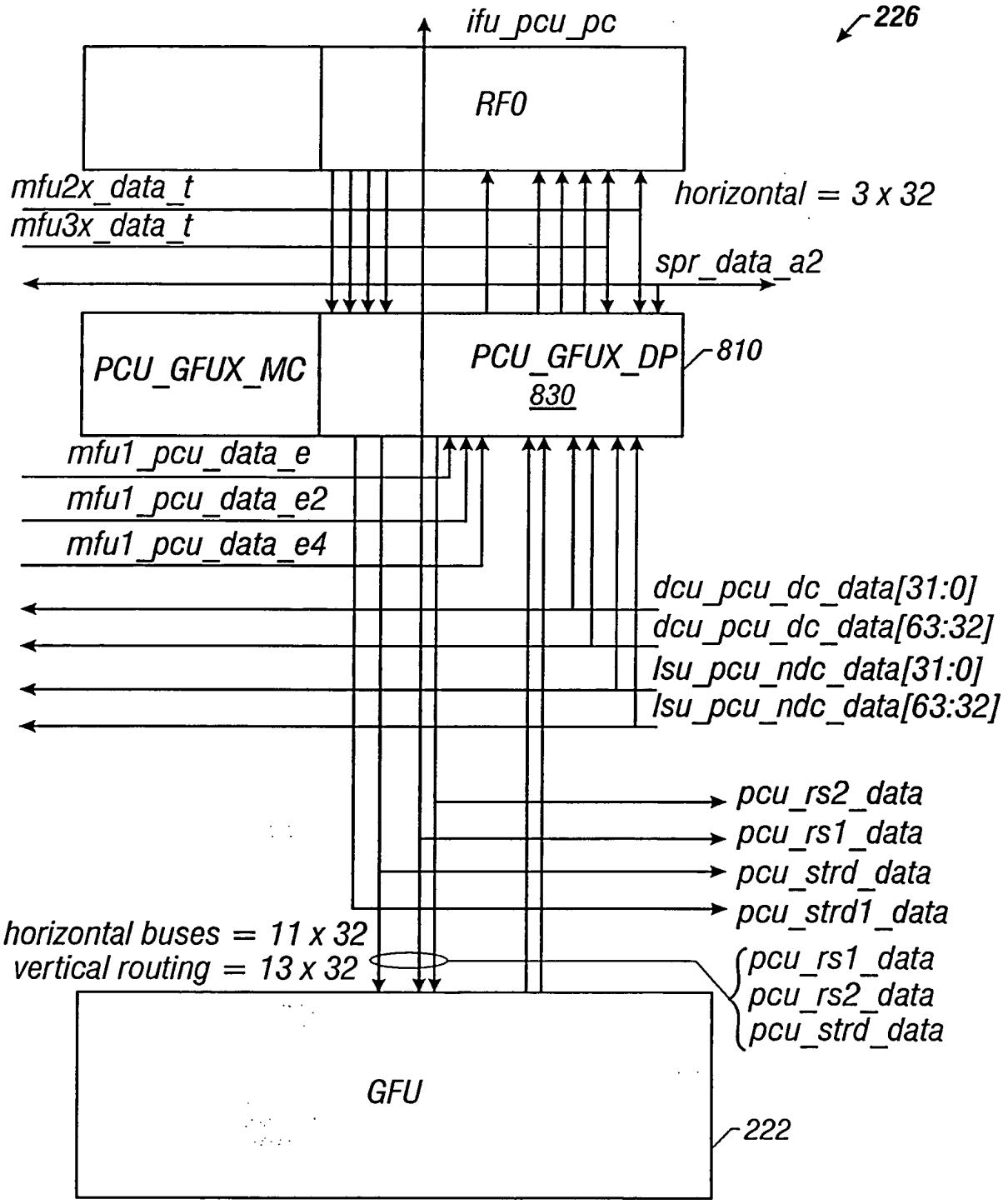
ifu_pcu_pc
226
RF0
mfu2x_data_t
mfu3x_data_t
horizontal = 3 x 32
spr_data_a2
PCU_GFUX_MC
PCU_GFUX_DP
830
810
mfu1_pcu_data_e
mfu1_pcu_data_e2
mfu1_pcu_data_e4
dcu_pcu_dc_data[31:0]
dcu_pcu_dc_data[63:32]
lsu_pcu_ndc_data[31:0]
lsu_pcu_ndc_data[63:32]
pcu_rs2_data
pcu_rs1_data
pcu_strd_data
pcu_strd1_data
horizontal buses = 11 x 32
vertical routing = 13 x 32
pcu_rs1_data
pcu_rs2_data
pcu_strd_data
GFU
222

FIG. 8A

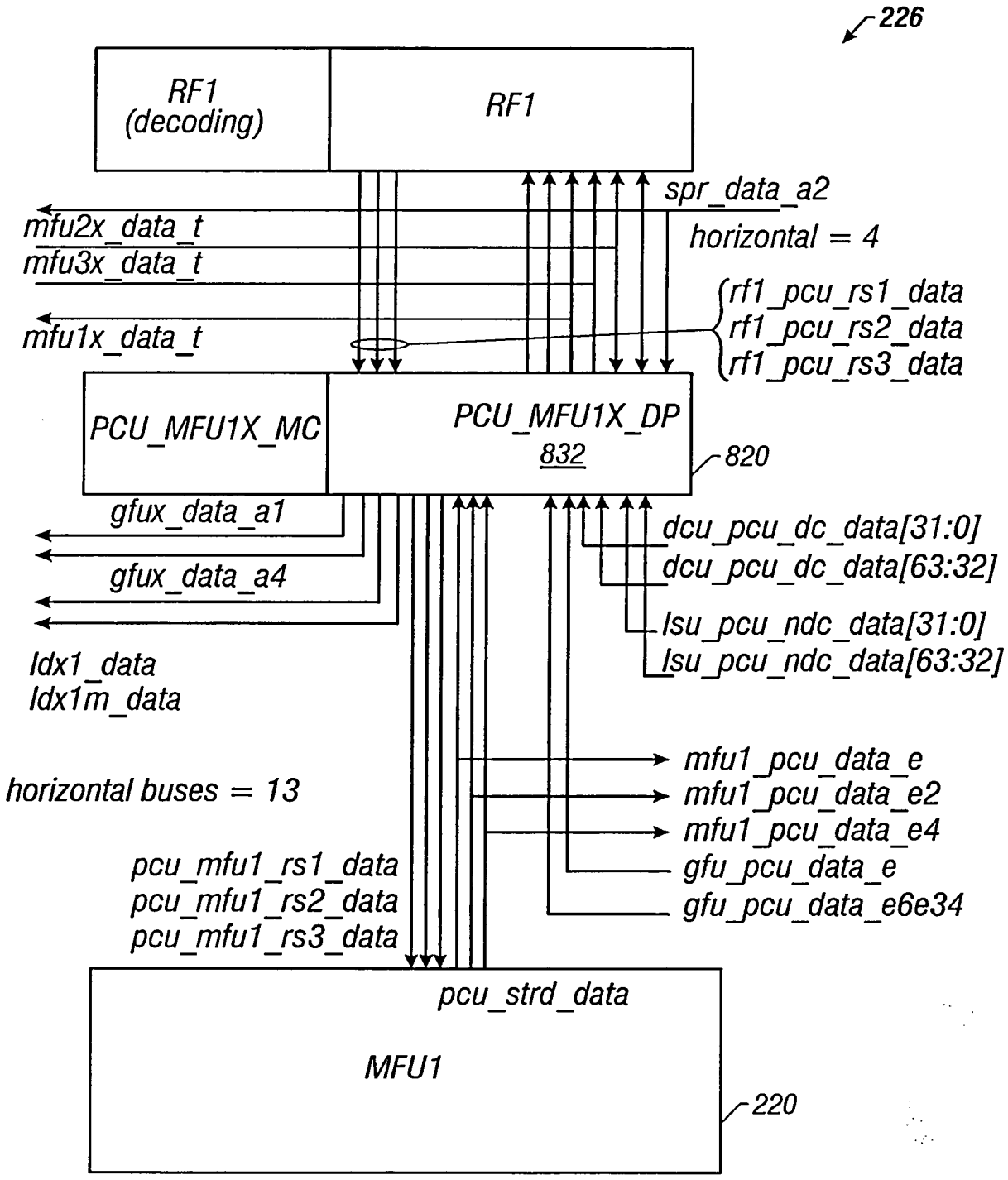
226
RF1 (decoding)
RF1
spr_data_a2
horizontal = 4
mfu2x_data_t
mfu3x_data_t
mfu1x_data_t
rf1_pcu_rs1_data
rf1_pcu_rs2_data
rf1_pcu_rs3_data
PCU_MFU1X_MC
PCU_MFU1X_DP
832
820
gfux_data_a1
gfux_data_a4
dcu_pcu_dc_data[31:0]
dcu_pcu_dc_data[63:32]
lsu_pcu_ndc_data[31:0]
lsu_pcu_ndc_data[63:32]
Idx1_data
Idx1m_data
horizontal buses = 13
mfu1_pcu_data_e
mfu1_pcu_data_e2
mfu1_pcu_data_e4
gfu_pcu_data_e
gfu_pcu_data_e6e34
pcu_mfu1_rs1_data
pcu_mfu1_rs2_data
pcu_mfu1_rs3_data
pcu_strd_data
MFU1
220

FIG. 8B

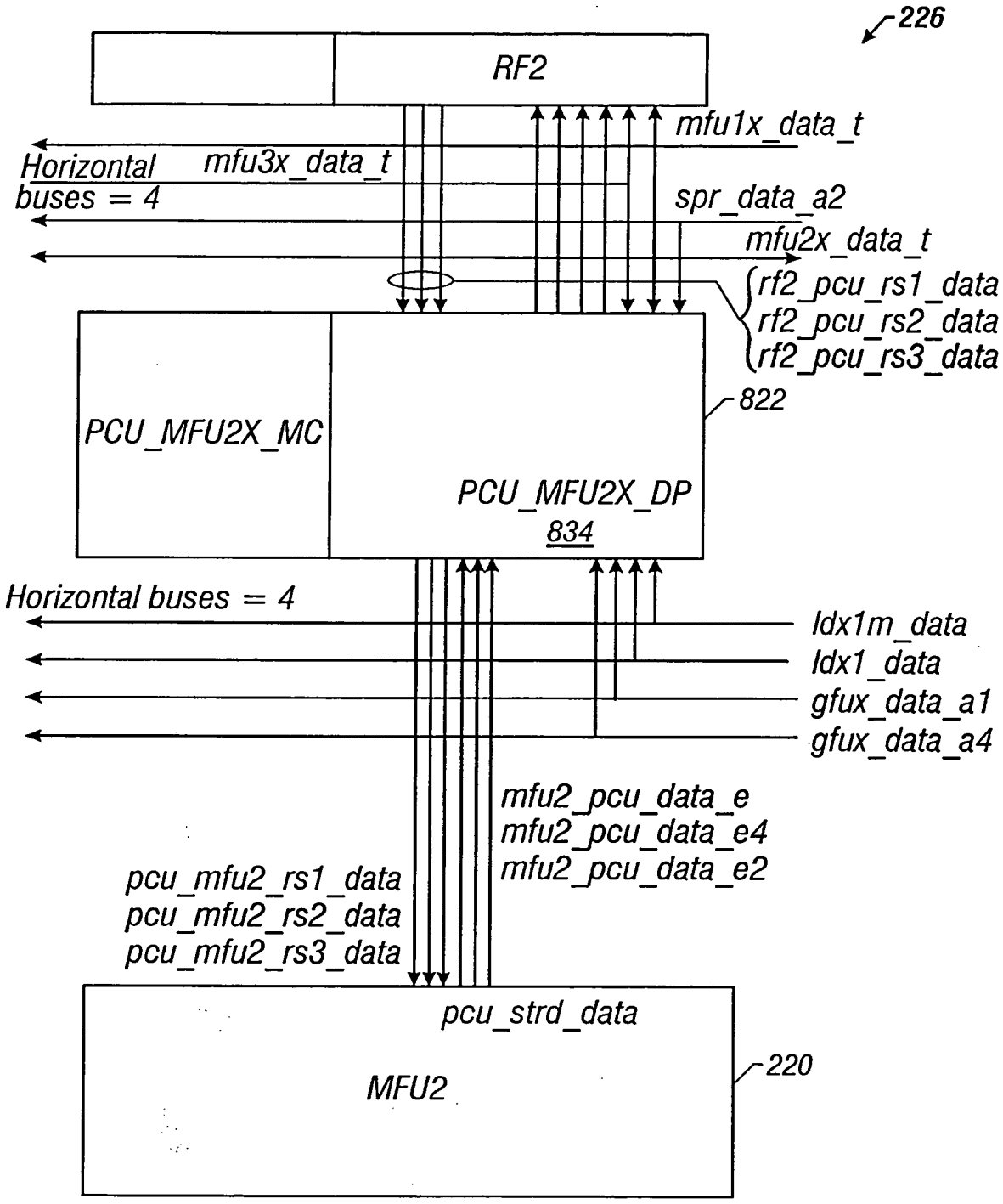
226
RF2
mfu1x_data_t
Horizontal buses = 4
mfu3x_data_t
spr_data_a2
mfu2x_data_t
rf2_pcu_rs1_data
rf2_pcu_rs2_data
rf2_pcu_rs3_data
822
PCU_MFU2X_MC
PCU_MFU2X_DP
834
Horizontal buses = 4
ldx1m_data
ldx1_data
gfux_data_a1
gfux_data_a4
mfu2_pcu_data_e
mfu2_pcu_data_e4
mfu2_pcu_data_e2
pcu_mfu2_rs1_data
pcu_mfu2_rs2_data
pcu_mfu2_rs3_data
pcu_strd_data
MFU2
220

FIG. 8C

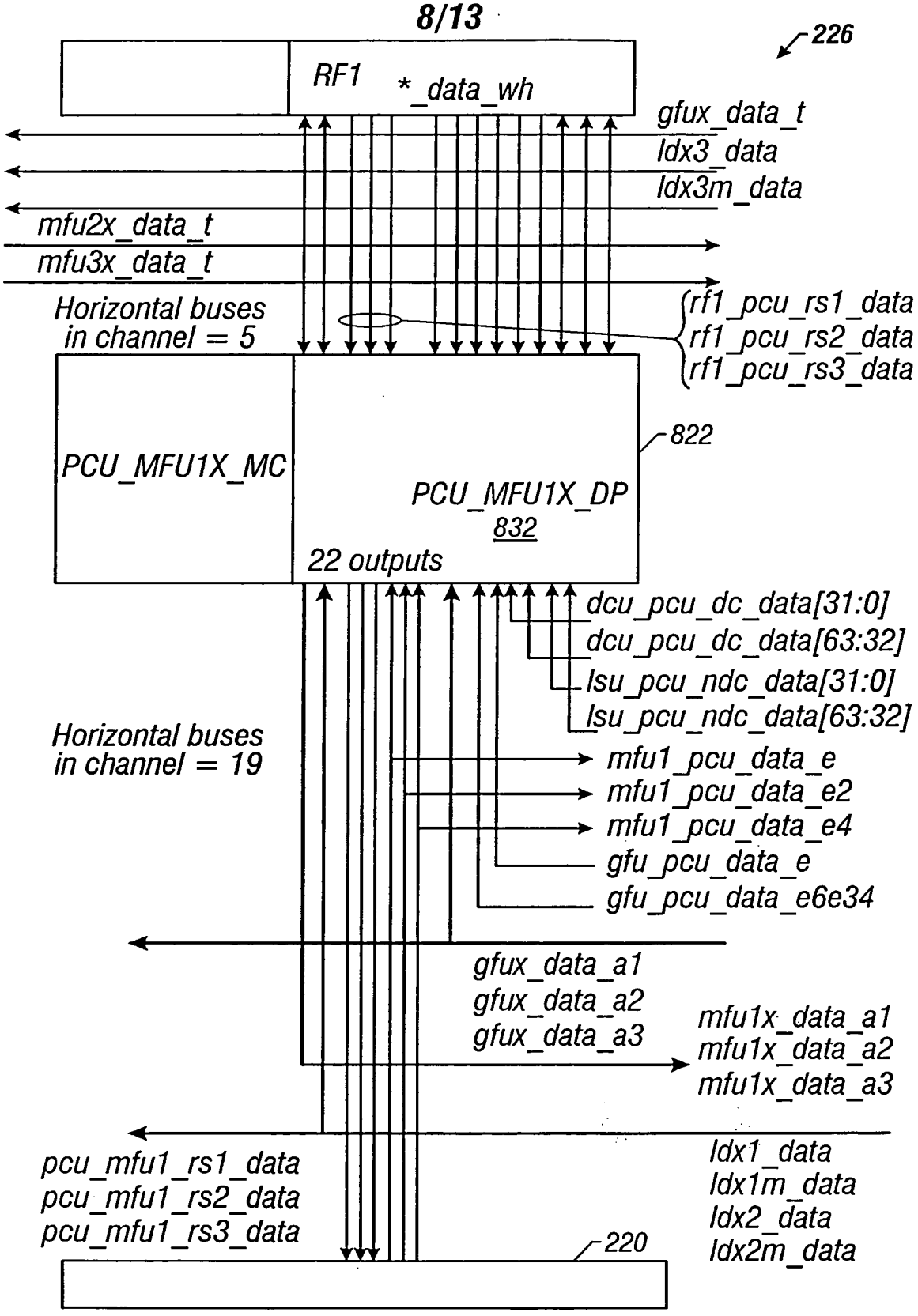
226
RF1
*_data_wh
gfux_data_t
ldx3_data
ldx3m_data
mfu2x_data_t
mfu3x_data_t
Horizontal buses in channel = 5
rf1_pcu_rs1_data
rf1_pcu_rs2_data
rf1_pcu_rs3_data
822
PCU_MFU1X_MC
PCU_MFU1X_DP
832
22 outputs
dcu_pcu_dc_data[31:0]
dcu_pcu_dc_data[63:32]
lsu_pcu_ndc_data[31:0]
lsu_pcu_ndc_data[63:32]
Horizontal buses in channel = 19
mfu1_pcu_data_e
mfu1_pcu_data_e2
mfu1_pcu_data_e4
gfu_pcu_data_e
gfu_pcu_data_e6e34
gfux_data_a1
gfux_data_a2
gfux_data_a3
mfu1x_data_a1
mfu1x_data_a2
mfu1x_data_a3
pcu_mfu1_rs1_data
pcu_mfu1_rs2_data
pcu_mfu1_rs3_data
ldx1_data
ldx1m_data
ldx2_data
ldx2m_data
220

FIG. 8D

Register name	width	address specifier	user access	supervisor access	thread state
PSR	8	010_0001	no	rd/wr	yes
TPSR1	8	010_0010	no	"	yes
TPSR2	8	010_0011	no	"	yes
PCR	7	010_0000	no	"	no
TL	2	010_0100	no	"	no
TICK	32	010_0101	read only	"	no
TVALUE	32	010_0110	no	"	no
TCNTL	8	010_0111	no	"	no
GX	13	001_0000	no	rd only	yes
INT	7	010_1000	no	rd/wr	yes
FSR	16	001_0001	rd/wr	"	yes
FMT	2	010_1010	rd/wr	rd/wr	yes
DIRTY	6	010_1011	rd/wr	"	yes
INT_OTHER	—	010_1001	no	wr only	yes

FIG. 9

PCR	PCR	Description	Initial value	After a trap
[0]	POW	power management	0 (off)	N/C not changed
[1]	ICE	icache enable	0	"
[2]	DCE	dcache enable	0	"
[3]	BPTE	branch predict taken enable	0	"
[4]	PE	pipeline enable	0	"
[5]	MSTEP	memory step	0	"
[6]	PID	processor ID	hardwired	hardwired

FIG. 10

Instruction	Instruction
vliw_1	setir ra, PSR
vliw_2	ld_2 [r1+r2], r3
vliw_3	ld_3
vliw_4	ld_4
vliw_5	ld_5
vliw_6	ld_6

FIG. 11A

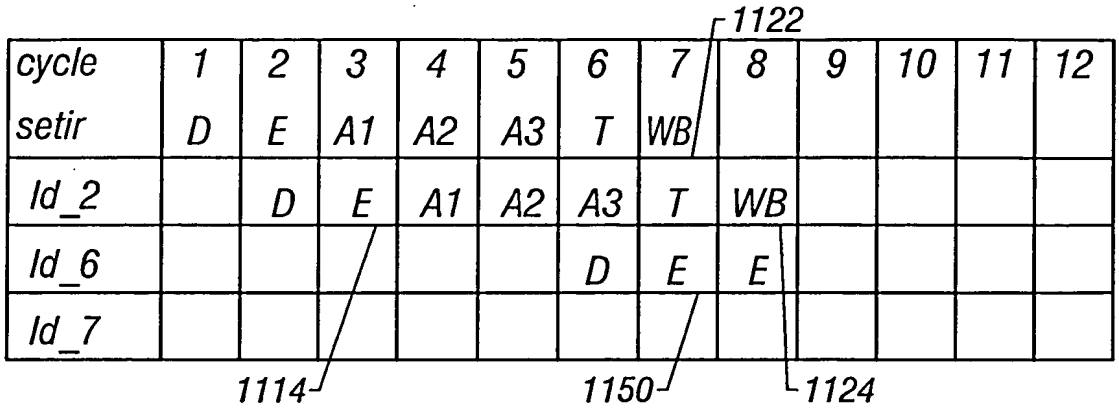

FIG. 11B

Instruction	Instruction
vliw_1	setir ra, PCR
vliw_2	inst 2
vliw_3	inst 3
vliw_4	inst 4
vliw_5	inst 5
vliw_6	inst 6
vliw_7	inst 7
vliw_8	inst 8
vliw_9	setir rb, PSR
vliw_10	inst 10
vliw_11	inst 11

FIG. 12A

1212 1222

cycle	1	2	3	4	5	6	7	8	9	10	11	12	13
setir	T	WB											
inst7		D	D	E	A1	A2	A3	T	WB				
inst8				D	D	D	D	D	D	D	E	A1	A2
setir											D	D	D
iST		ST		ST	ST	ST	ST	ST	ST		ST	ST	ST

1254

cycle	14	15	16	17	18	19	20	21	22	23	24	25	26
inst8	A3	T	WB										
setir	D	D	D	D	E	A1	A2	A3	T	WB			
inst10					D	D	D	D	D	D	E	A1	A2
inst11											D	E	A1
ST	ST	ST	ST		ST	ST	ST	ST	ST				

FIG. 12B

1300

Instruction	Unit	rd [6:5]
[0]	all	01
[1]	all	10
[2]	gfu	11
[3]	mfu1	11
[4]	mfu2	11
[5]	mfu3	11

FIG. 13

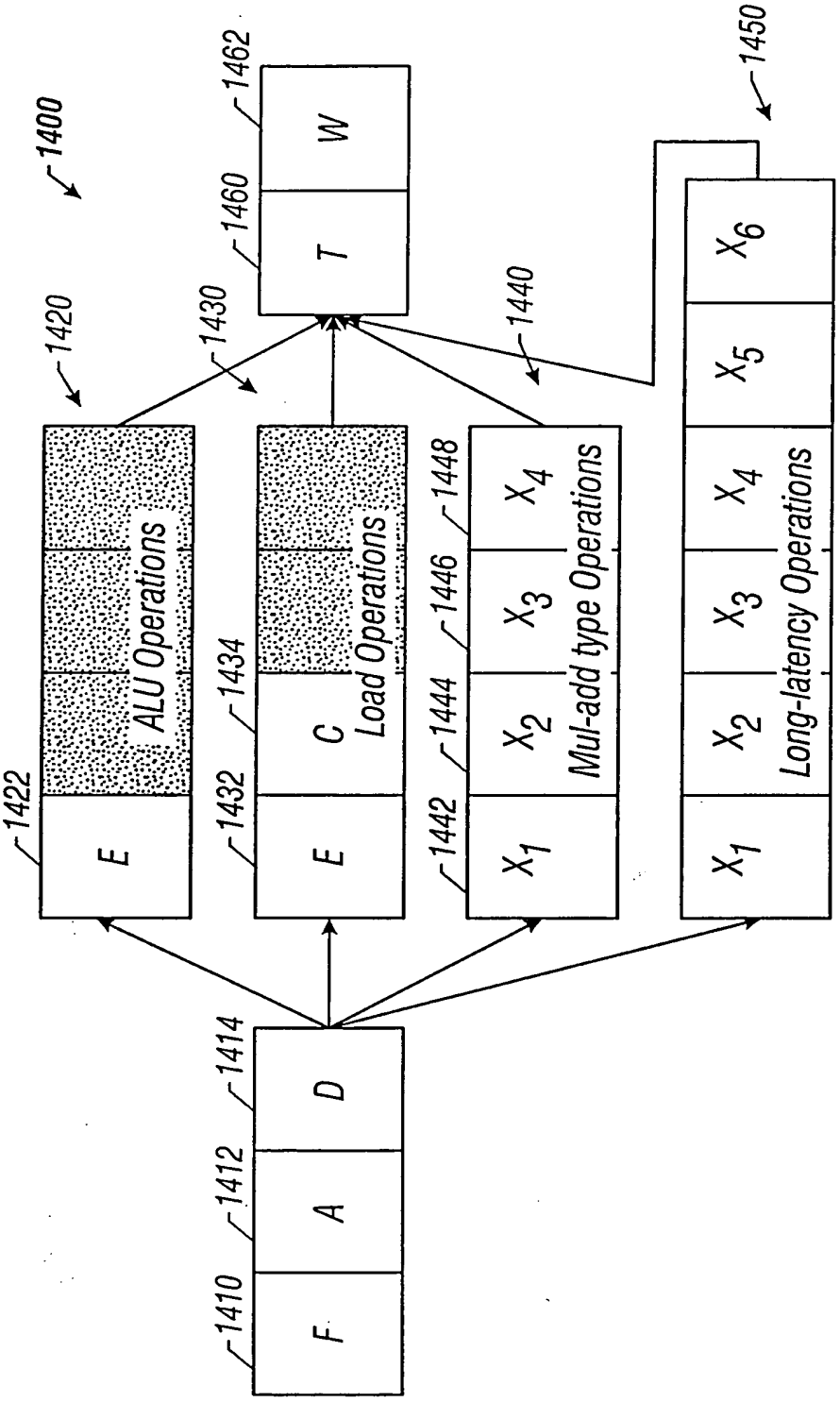
1400
1410
F
1412
A
1414
D
1420
1422
E
ALU Operations
1430
1432
E
1434
C
Load Operations
1440
1442
X1
1444
X2
1446
X3
1448
X4
Mul-add type Operations
1450
1460
T
1462
W
X1
X2
X3
X4
X5
X6
Long-latency Operations

FIG. 14